Ed Note: This article first appeared in Printed Circuit Design Magazine in July, 2000. I have always considered it a classic. While it is written from the relatively narrow aspect of "controlling EMI," the conclusions re board stack-up have relevance for almost all signal integrity issues, from EMI to Crosstalk to Power Distribution Systems (i.e. bypass capacitors). The bottom line conclusion is (1) route every trace directly over and close to a related, continuous plane, and (2) provide at least one Pwr/Gnd planar pair for planar capacitance. It is reprinted here on our web pages by permission. Doug Brooks

Controlling Radiated EMI Through PCB Stack-up
Rick Hartley

There's more than one way to skin a cat and even more ways to battle EMI, beginning at one of the most basic levels of PCB design.

Clearly there are a number of circuit and PCB design techniques that designers and engineers need to master in order to control high-frequency, radiated EMI. It's fairly well understood that circuit board stack-up can play a major role in the effort to control EMI. A good stack-up helps to contain electric and magnetic fields and is a very strong aid in the effort to bypass/decouple the power bus. This article will examine these issues and detail several board stack-ups designed to accomplish these goals.

The power bus

When an IC is clocked and its outputs drive multiple transmission lines, the outputs are both a changing voltage and a changing current. The energy for these changing outputs comes from the system's power structure. An issue that's well understood by most designers and engineers is that the energy needed to drive the IC outputs does not come directly from the power system's power supply. Due to inductance of the power bus, even a power supply that is only a few inches away from an IC cannot deliver the energy quickly enough for the output transitions to occur in the short time needed. This, of course, is where bypassing/decoupling capacitors come into play.

By strategically placing properly sized capacitors at the power pins of the ICs, we are able to help provide some of the energy to the ICs quickly enough to allow the fast output transitions to occur. But wait; that's not all. Unfortunately, the capacitors have a limited frequency response, which keeps them from delivering power at all the frequencies needed to create the harmonics necessary to cleanly drive the IC's outputs. To compound the problem, the transients that develop on the power bus, due to voltage drops across the inductance in the decoupling paths, are major sources of common-mode EMI. So what do we do?

To an IC in our circuit, the area of the power planes near the IC looks like a good, high-frequency capacitor and will pick up where the discrete capacitors fall off by providing the high-frequency energy needed for clean outputs. Additionally, a good set of power planes are low in inductance, hence the transients that develop are much lower, causing lower common-mode EMI.

Of course, connection of the power planes to the IC power pins must be right next to the IC pins and as rise times get faster, the connection will need to be in the pads of the IC power pins. But that's a topic for another article.

For the planes to help with decoupling and for them to be low enough in inductance to help control common-mode EMI, they must be a very good set of planes. How good is very good? The answer to that question is a function of plane separation, the material between the planes, and frequency (hence a function of IC rise time). A normal set of planes .006 inch apart, with FR4 between them, have approximately 75 pF of capacitance per square inch of plane area. Of course, the closer the planes are to one another, the higher the capacitance. Normal planes separated by .003 inch have about 150 pF of capacitance per square inch. In both of these cases, "normal planes" means planes broken up by holes from vias and holes from component leads. After all, in the real world, planes are almost never solid, undisturbed copper.

A few of today's devices have rise times of 100 to 300 ps. At the rate of progression of ICs, a high percentage of tomorrow's devices will have rise times in that range. In circuits with 100 to 300 ps rise times, even planes with 3 mils separation probably won't be adequate in most cases. In this scenario, it will likely become necessary to have planes separated by well under 1 mil, with dielectric materials other than FR4—dielectric materials with very high permittivity. Ceramics and ce-

ramic-loaded plastics are some of the materials currently used for this purpose (This too is the topic of another article).

Even though tomorrow will probably bring new materials and new methods, with today's commonly seen 1- to 3-ns rise times, those 3- to 6-mil separated planes, with FR4 between them, are usually adequate to handle the high-end harmonics and keep transients low enough to dramatically lower common-mode EMI. The PCB stack-ups defined in this article will assume the use of planes at a spacing of between 3 and 6 mils.

Field containment

To truly control radiated EMI, it's essential to contain the electric fields and the magnetic fields generated within a circuit. To control and contain these fields requires an understanding of how they originate.

For every outgoing current there is an equal but opposite polarity return current. All circuit currents travel in pairs. Always think about both voltage and current in pairs and provide both a forward path and a return path. This pair of paths need to be high in capacitance and low in inductance. High capacitance between a forward signal and its return path means good containment of the electric field. Low inductance of the pair means good flux cancellation, hence good control or containment of the magnetic field.

In a circuit board, this high capacitance/low inductance environment is ideally created when a forward current is completely surrounded by its return current, totally containing both the electric and magnetic fields. An ideal setting would also have a balanced impedance between the forward path and the return path.

From the perspective of signal routing, to balance the paths and totally contain the fields we would need to run all signals in twisted, shielded pair cables. Of course, this is not practical in a printed circuit board. Very sensitive signals in a circuit board can, on an individual basis, be routed in a pseudo-twisted-pair fashion, but this requires a great deal of effort and is not a practical solution for all signals.

The next most ideal setting is a coaxial cable. Coaxial cables don't have ideal balance between the forward and return paths, but they do provide complete containment of the fields when connected properly. In a circuit board, a structure very closely resembling a coax can be created by centering a signal between two ground layers with a wide ground trace on either side and connecting the ground layers and the wide ground traces with vias every 1/20 wavelength, as illustrated in the cutaway view in Figure 1.
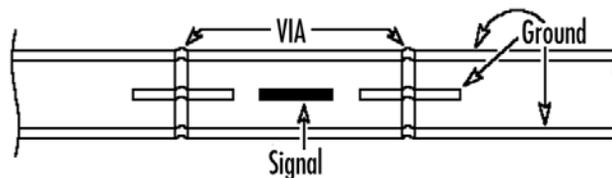

Figure 1 - Signal trace routed as a pseudo-coax

This is all very nice, but in a high-density digital design, the opportunity to place a ground trace on both sides of every signal trace is just about nonexistent. However, placing signals in layer pairs, routed perpendicularly to each other and placed close to a reference plane(s), is a very realistic possibility. This might not represent an "ideal" coax, but will certainly go a long way toward achieving the goal of true field containment.

For power and ground currents, an ideal setting would have each power current completely surrounded by its return current (ground). If the power currents are in a plane, how is that possible? Ideally, it's not. But the concept can be basically achieved by placing the power plane between two ground planes. This may be a nearly ideal set-

ting for containment of the fields associated with power currents, but it's likely to be a problem during fabrication of the bare board. Fabricators need balanced construction, and three planes together anywhere in a board stack is not balanced construction.

All right, so we know what's ideal, but we also know that what's ideal cannot be achieved in a cost-effective manner. So what do we do? From the perspective of signal traces, a very good setting can be created by routing all signals on the layer or layers next to a plane (power or ground). In the case of power currents, a very good environment is created by placing the power plane right next to a ground plane and very close together. This is the "set of planes" discussed in the previous section.

Board stack-up

So which board stack-ups achieve the goals of good field containment and provide a very good set of planes and which board stack-ups fly in the face of success? The following stack-ups assume all power currents are on a single layer, either one voltage or multiple voltages on a segmented plane. The case of multiple power planes is discussed later.

Four-layer boards

A four-layer design has several potential problems. First, a conventional .062-inch-thick, four-layer board, with signals on outer layers and planes on inner layers, has a wide separation between the power and ground planes. This large separation is a natural byproduct of foil lamination (the process used by fabricators to manufacture most bare PCBs). In a foil-laminated board, the fabricator starts with an inner core in the range of 25 to 40 mils thick, processes the core (print and etch, etc.), and then stacks prepreg on either side of the core, followed by a copper foil sheet on either side of the prepreg. In this case the core has to be thick to keep the prepregs fairly thin. Otherwise, fabricating a flat board can be very difficult.

A board can be fabricated using core lamination (two cores with prepreg in the center), so that power and ground can be tightly spaced in the center. But then the signal routes will be so far away from the planes (in a .062-inch-thick board) that differential-mode EMI will be severely increased. There are those who would argue that an increase in differential-mode EMI is not as severe as high levels of common-mode EMI. This may be an accurate statement, but because of the increased inner layer processing time, a core-laminated four-layer board would cost as much, or nearly as much, as a foil-laminated six-layer design.

For the reasons stated, it makes no economic sense to buy a core-laminated board. If you're going to pay for six layers, buy six layers, not four. If economy is a major concern, two alternatives to a conventional four-layer board are shown in Figure 2. These stack-ups will offer some improvement in performance, but only if the component density on the board is low enough to allow good planes to be poured around the components.
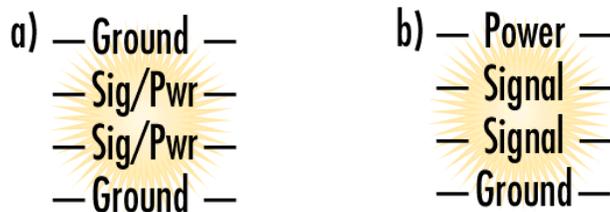

Figure 2 - Better four-layer designs

The stack-up in Figure 2a (power-routed with wide traces, in a grid on the signal layers) is preferred because it provides a low impedance path for power currents as well as a low impedance, stripline path for signals. From a standpoint of EMI control, this is the best four-layer PCB available. The stack-up in Figure 2b is a minor improvement over the conventional four-layer board, but like the conventional four-layer board, it does not offer a good set of low impedance planes.

If control of trace impedance is necessary, both these stack-ups require very careful routing of traces to keep them under the islands of poured power and ground. Also, the poured islands on layer 1 (power or ground) must be tied together in as many places as possible to maximize the DC and low-frequency connectivity. This is also true for layer 4 (ground).

Six-layer boards

If component density on the board is high enough that quality planes cannot be poured, the most reasonable alternative is a six-layer board. Some board stacks do far less to contain fields, help the power bus and lower transients than others. Figure 3 shows two such board stacks.
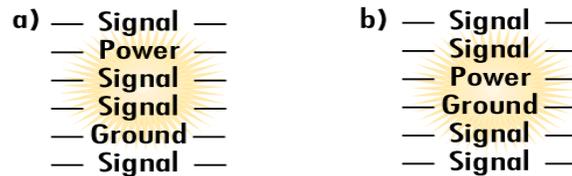

a)
— Signal —
— Power —
— Signal —
— Signal —
— Ground —
— Signal —

b)
— Signal —
— Signal —
— Power —
— Ground —
— Signal —
— Signal —

Figure 3 - Six-layer designs to avoid

The stack-up in Figure 3a is a severe detriment to the control of radiated, common-mode EMI, due to high plane impedance. It is great from the standpoint of impedance control of signals and is therefore recommended by some IC manufacturers for high signal integrity in the board. But, as indicated, it is a problem for EMI.

The design in Figure 3b solves the problem of plane impedance but is a concern because of increased differential-mode EMI, due to poor field containment of layers 1 and 6. Figure 3b can be made to work if the outer layer routes are minimized in number and kept very short (less than 1/20 the wavelength of the maximum harmonic frequency of the signals). This works especially well when the open space on the outer layers is poured with copper fill and the copper is grounded (every 1/20 wavelength preferred). As before, connect the poured copper together and to the internal ground plane in multiple places. Two examples of high-performance six-layer designs are shown in Figure 4. The layout in Figure 4a would be ideal as a very good general design. Nothing could be quieter than two centered stripline signal layers, with a centered power and ground pair. Obviously, the down side to this design is that it has only two routing layers. As explained, this same stack-up is achieved with a conventional six-layer board when the outer layer traces are kept short and copper is poured in the open areas.
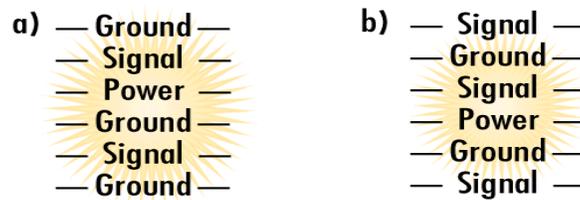

a)
— Ground —
— Signal —
— Power —
— Ground —
— Signal —
— Ground —

b)
— Signal —
— Ground —
— Signal —
— Power —
— Ground —
— Signal —

Figure 4 - High-integrity six-layer designs

The layout in Figure 4b also represents a very good environment for high signal integrity. Each signal layer is adjacent to a ground layer and the board has a power and ground pair. Obviously, the down side is the imbalance in the layer stacking.

This is usually a problem for fabricators. The way to avoid problems with fabrication is to pour copper fill in all

open areas of layer 3. If, after copper fill, layer 3 has the approximate copper density of the planes, the board will be a balanced construction. Copper fills must connect to ground or power. A connecting via to ground every 1/20 wavelength is ideal—not usually possible, but ideal.

Eight-layer boards

Signal quality and EMI control start to take on high-end qualities in six-layer designs, but really begin to excel at eight layers and up. Before discussing eight-layer stack-ups that work well, let's examine some board stacks to avoid. Figure 5 shows three boards that can create severe EMI problems.
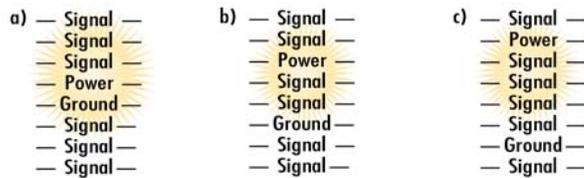

Figure 5 - Eight-layer designs to avoid

The conventional eight-layer design, with six-signal layers (no matter how they are stacked), is not recommended. It goes without saying that none of the designs in Figure 5 can provide low levels of both differential-mode and common-mode EMI. The stack in Figure 5a could be made to work if all the signals on layers 1 and 8 were few and very short and the open area of these layers was poured with grounded copper. Handled in this way, Figure 5a looks very much like Figure 6a. Figure 5b and Figure 5c have virtually no redeeming value.

Two examples of high-performance eight-layer designs are shown in Figure 6. The layout in Figure 6a is a good general design, with offset stripline signal layers and a centered power and ground pair. The layout in Figure 6b is the more ideal of the two. The reasons for this are explained in the following paragraphs.

Figure 6 - High-integrity eight-layer designs
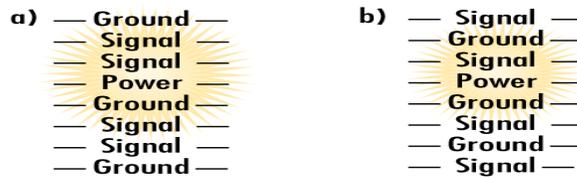
Ten-layer boards

Due to the very thin dielectrics in high-layer-count boards, those of the 10- and 12-layer variety have extremely low plane impedance and excellent signal quality, if properly stacked. In a .062-inch-thick board, 12 layers become more difficult to fabricate and will severely limit the number of fabricators able to make the bare board.

Since signal layers should always be routed one dielectric layer away from a return plane, having more than six signal layers in a 10-layer stack-up is not a good idea. Also, placement of the signal layers relative to the planes is very important. The 10-layer stack in Figure 7 is a nearly ideal environment.
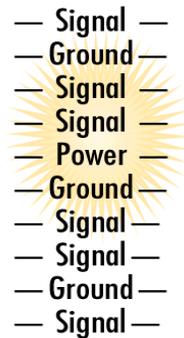
Figure 7 - High-integrity 10-layer design

In addition to the good set of tightly coupled planes in the center of the board, the reasons this 10-layer design and the eight-layer in Figure 6b are ideal environments has to do with the coupling of signal and return currents. Let's examine the concept using the 10-layer design. Properly structured, layer 1 would route in the X direction, layer 3 in the Y direction, layer 4 in the X direction, etc. From the perspective of trace routing, layers 1 and 3 are a layer pair, layers 4 and 7 are a layer pair and layers 8 and 10 are the remaining layer pair. All signals routed on layer 1 should be "via'd" to layer 3 when a direction change is necessary. This may not always be possible, but the concept should be followed as closely as possible.

Likewise, all signals on layer 8 should via to layer 10 for a direction change. The layer 4 and 7 pair should get the same treatment. This approach to routing ensures that every forward signal will always be coupled very tightly with its complement (return). For example, if a signal is traveling on layer 1, its return current will be in the plane on layer 2 and only layer 2. If that signal vias to layer 3, its return stays in the layer 2 plane, maintaining low inductance, high capacitance and good field containment.

What happens if this approach is not maintained? If the same signal is traveling on layer 1 and it vias to layer 10, the return current must now find a path to the ground plane on layer 9. The return current will have to find the nearest ground via (i.e., resistor or capacitor lead to ground). If that via happens to be nearby, that's OK. If a ground via is not nearby, the inductance increases, capacitance decreases and EMI will increase.

The approach to take, when a signal must via to a layer outside its present layer pair, is to place a ground via right next to the signal via. This will provide a path for the return current to the appropriate ground layer. The suggested eight- and 10-layer designs are best for this approach because they allow for easy layer pairing with the fewest number of needed ground vias to maintain good signal coupling. In the case of the layer 4 and 7 pair, return currents will travel well in both the power and ground planes on layers 5 and 6, transferring easily between these two plane layers because of the good capacitive coupling between the planes.

Multiple voltage planes

If two planes of the same drive voltage (Vcc) are required to handle high amounts of power current, place two different sets of power and ground planes in the board. In this case, each plane pair is set up to always place power one dielectric layer away from the ground. This arrangement creates two equal impedance power buses that will split the current equally, as intended. If the board is stacked with power planes other than in equal impedance pairs, the current won't split equally and the voltage transients in the planes will be much larger, dramatically increasing EMI.

If the design has so many different voltages that more than one power plane is needed to segment them, remember that more than one set of plane pairs should be created. In both of these cases, when determining the location of plane pairs in the board, always remember that fabricators need balanced construction.

Summary

Since the vast majority of the designers and engineers designing circuit boards utilize conventional .062-inch-thick boards without blind or buried vias, all the board stack-ups discussed in this article assume those conditions. Some of the suggested stack-ups may not be ideal for boards whose thickness is greatly different. Likewise, due to the fabrication techniques used on blind and/or buried via boards, these stack-ups may not work there either.

Regardless of thickness, via technology or layer count, plan the board stack-up so that it will assist the bypassing/ decoupling of the power bus, minimize voltage transients on planes and contain the electric and magnetic fields of both signals and power. Ideally, this means traces should be routed one dielectric layer away from a return path and the pair of planes (or pairs of planes) need to be very tightly spaced. Following these basic concepts will allow you to create a board that always meets the desired goals. With IC rise times already very fast and getting faster, these techniques become necessary to meet the need to contain EMI.

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